Hierarchical Power Intent Driven Efficient Power Integration Methodology for Ultra Low Power Mixed-Signal SoC

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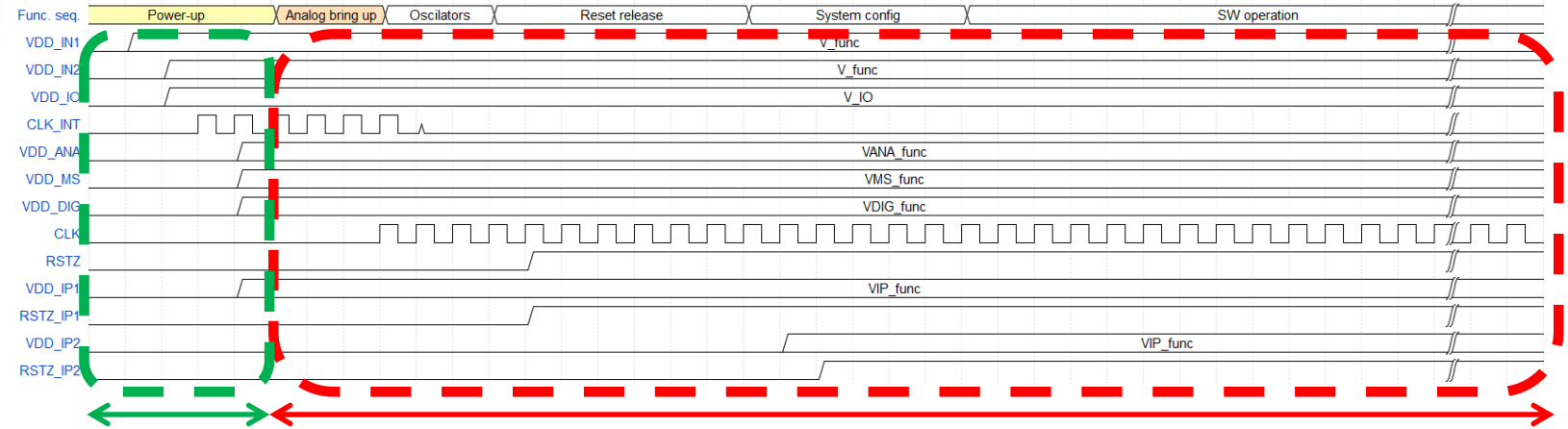
Motivation & Problem Statement

- Increasing functional complexity on mixed-signal (MS) SoCs
- Need for achieving lowest power consumption, compressed time to market
- Newly evolving ultra-low power SoC architectures require highly complex on chip power management (PM)
- Various levels of PM requirements → Architectural, structural and electrical
- Existing methods of SoC PI capture are effective, but inefficient → Manual, error prone and time consuming
- Necessitates robust power intent (PI) specification, PM integration, implementation and verification methods
- Should be consistent at all levels → Library components, IPs (Soft, Hard, digital & MSIPs) and SoC

Integration and Verification Challenges

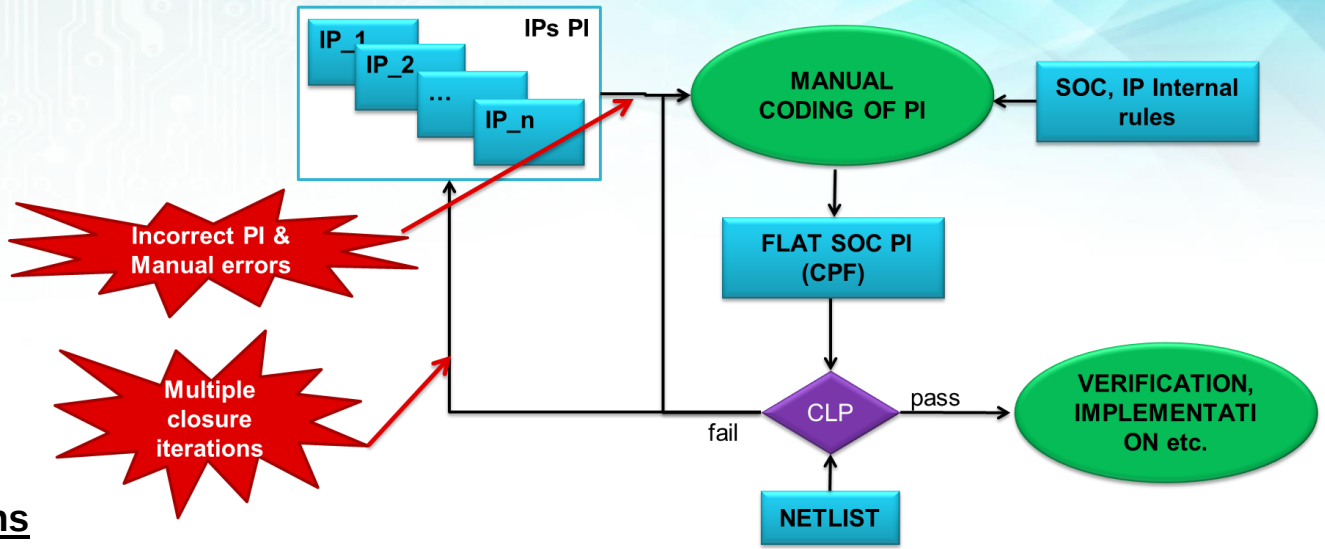
- Low power (LP) methodology formalized only at SoC toplevel ➔ Custom handled at IP level including complex MSIPs
- Significant differences between PIs used for implementation and verification
- Quality gaps & execution bottleneck due to absence of phased, reusable and hierarchical LP implementation and verification
- Power up sequence & verification criticality



Considered AON for implementation
→ **Verification is critical**

Complete Power modes considered for SoC implementation

Current Low Power Design Methodology



Limitations

- IPs developed and verified for functionality only ➔ PPA & schedule surprise after SoC integration
- Issue with low power cells in IP ➔ Late IP changes
- MSIP cannot be verified until its internal digital is implemented ➔ Delays in MSIP focused verification

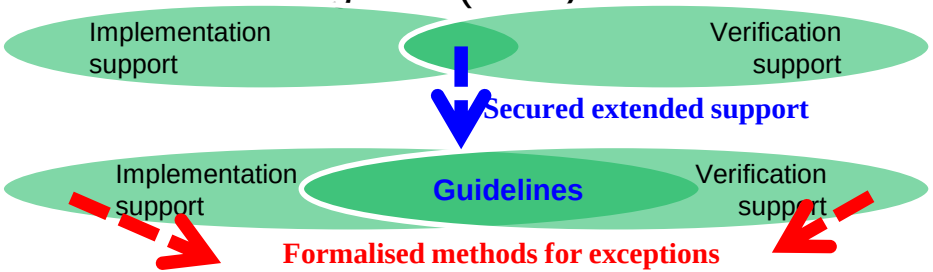
Proposed Solution & Methodology Overview

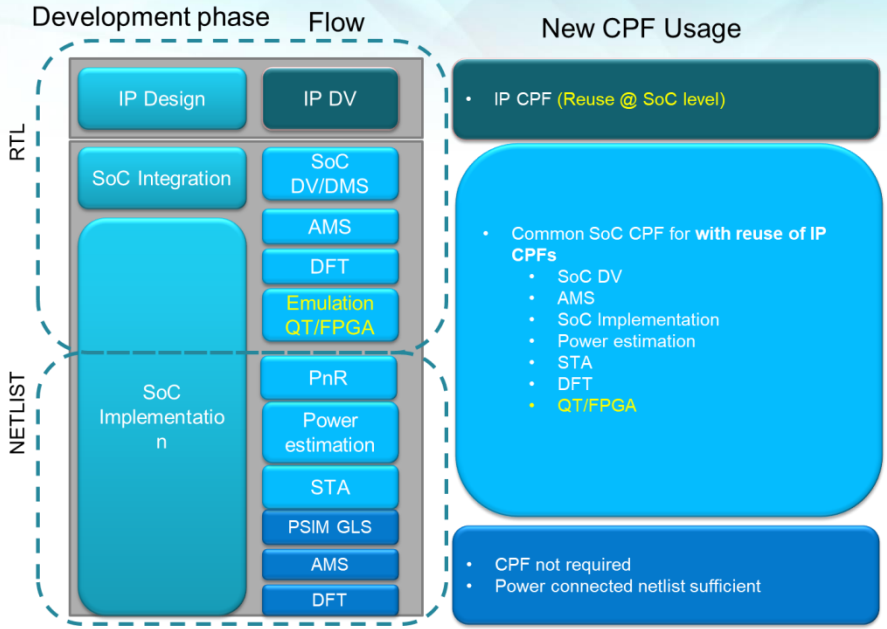
Goal: Efficient, hierarchical and reusable power intent driven low power implementation and verification methodology

1. Comprehend architectural intent in the power description
   - Custom isolation insertion requirement in addition to other low power design complexities
   - Custom design & integration steps
   - Tool enhancements for CLP check, integration, and low power mixed-signal simulation
2. Single standard, uniform PI across flows
3. Develop IP power intent
4. Develop SoC power intent
5. Standardised PI use model across flows

2. Single Standard, Uniform PI across Flows

- Logical connectivity is fully automated and mature using standard HDLs
- Power connectivity and intent
  - Independent parsers for various flows/tools
  - Difficult to capture flat SoC PI, automate and maintain consistency
  - Standard common power format is required
- Different PI formats & choice
  - Choice between IEEE 1801 (UPF) and CPF
  - Used CPF due to better maturity of tools and flows
  - Limitations with some PI constructs across tools
- Enabled single PI (CPF) across flows

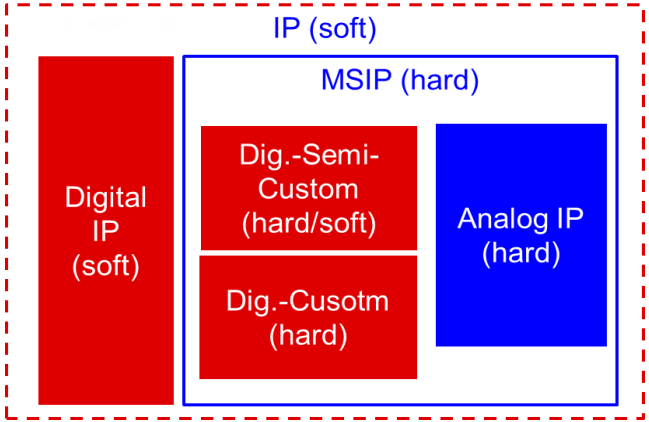




3. Develop IP Power Intent

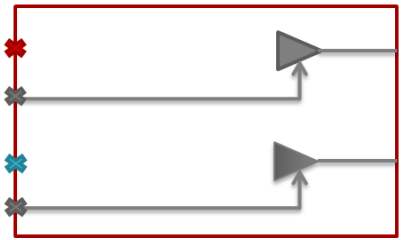
- "Constrained" power intent strategy for IPs to meet
  - Architectural constraints → Boundary port association, power modes, rules, etc.
- Enabling early SoC verification with Design CPF of hard IPs

MSIP integration context



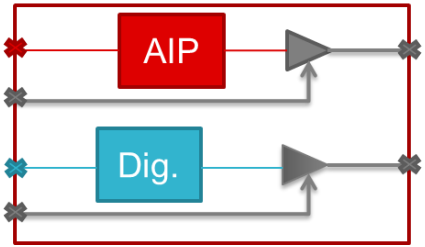
CPF flavours

Macro CPF view



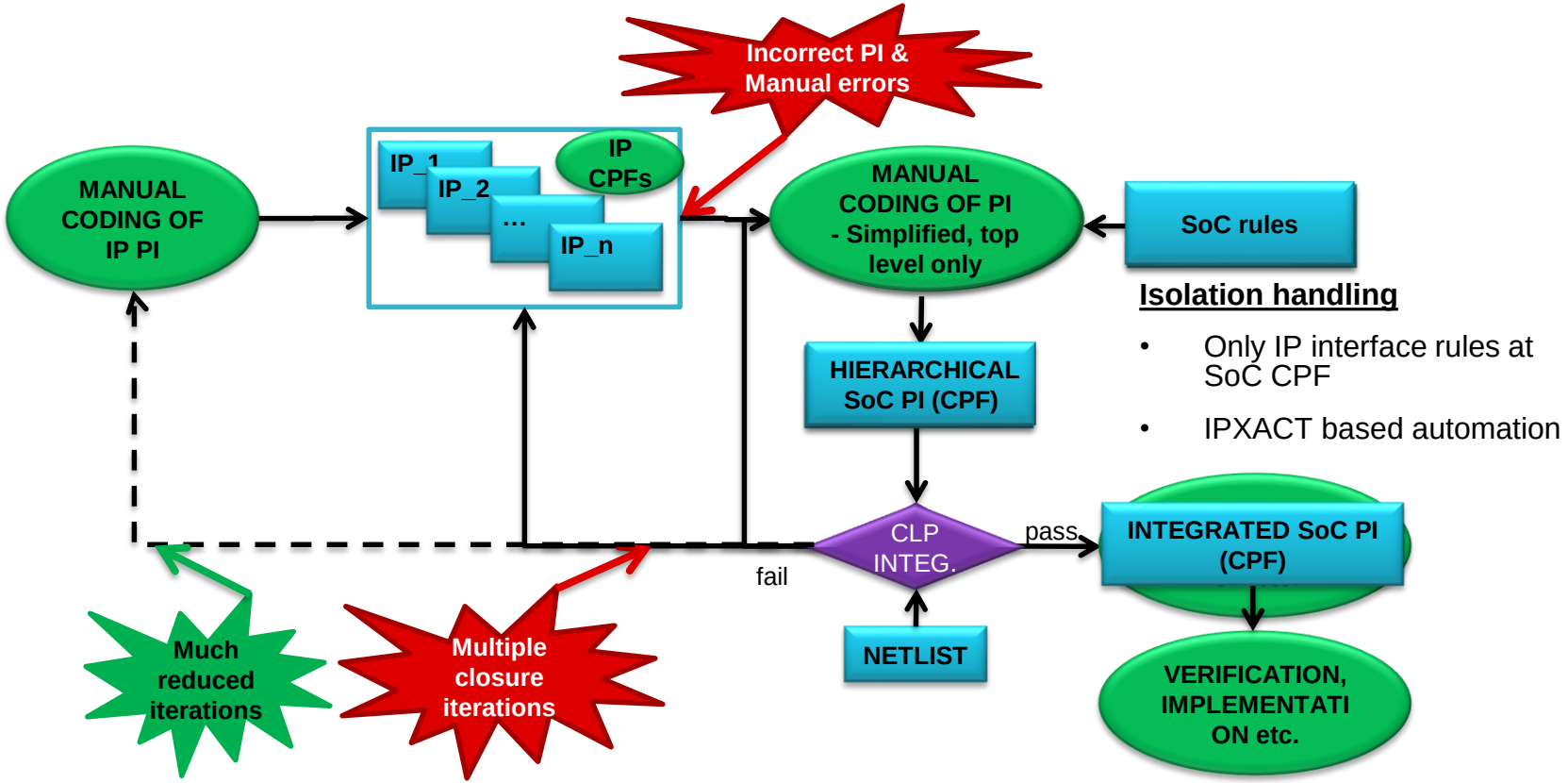
- For SoC Implementation
- IP & SoC verification: RTL DV/DMS/AMS + Dig. **GL** (Late)

Design CPF view

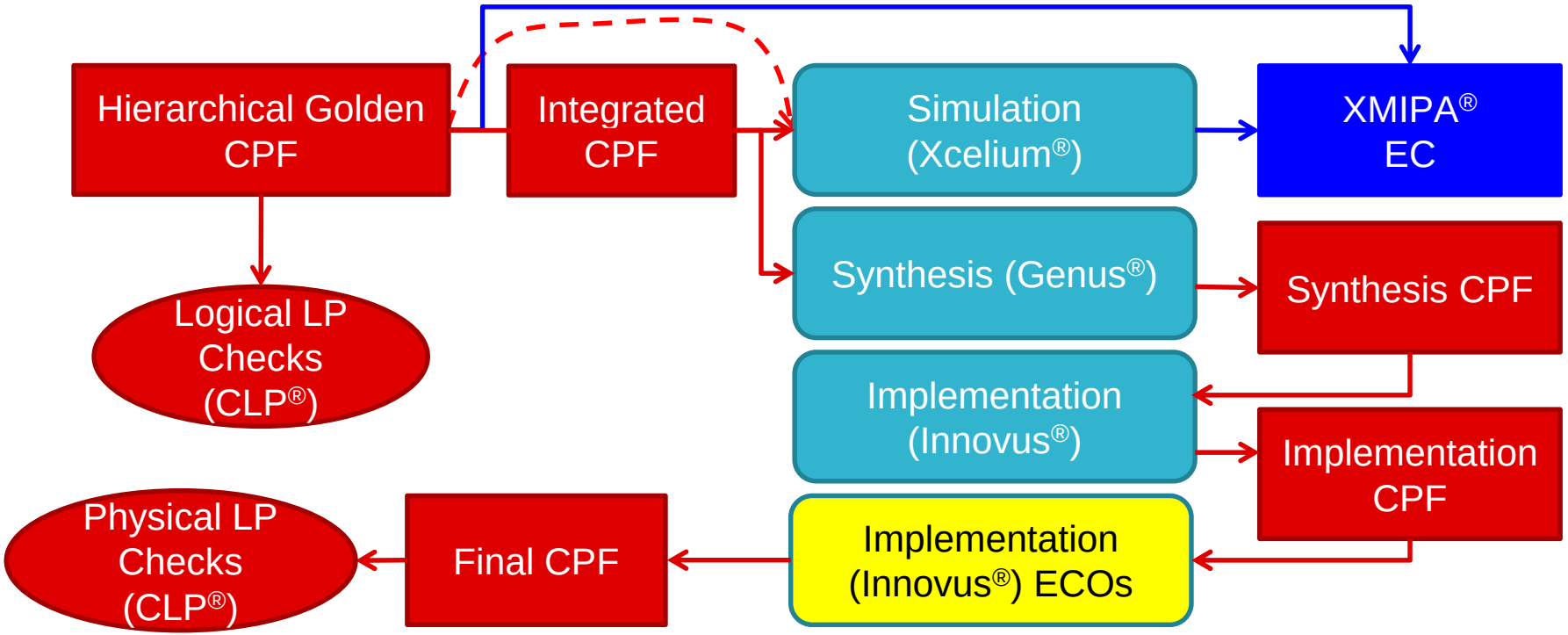


- For MSIP Implementation
- IP & SoC verification: RTL DV/DMS/AMS + Dig. **RTL** (Available early)

4. Develop SoC Power Intent



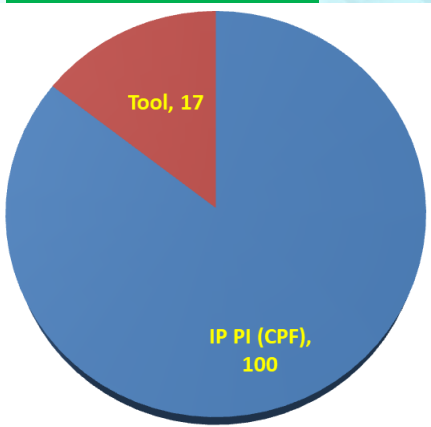
5. Standard PI Use Model across Flows



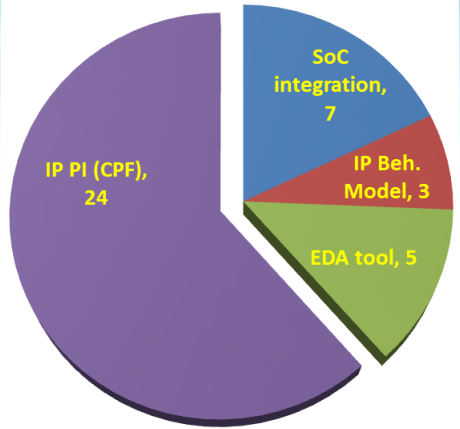
Evidence

- Proposed Hierarchical PI (CPF) approach applied on low power mixed-signal SoC development enabled
  - Independent & timely IP maturity before SoC
  - Methodology & tool enhancements in collaboration with Cadence
  - Early verification using Design CPF of MSIPs
  - Validated integrated CPF ➔ Through CLP based PI integration
  - Early verification before synthesis ➔ Through Logical RTL based CLP check
  - PA RTL DV quality improvement & correlation to implementation ➔ Through XMIPA® (LPS EC)
- Baseline methodology applied for MS SoC platform development
  - Early identification of design and integration issues
- Improvement in SoC PI capture complexity (10x) and Cycle times

CLP check statistics
Static PI



LP DV statistics
Dynamic PI correctness



PI complexity reduction

SoC PI complexity reduction			
	Number of lines of PI code		SOC PI capture complexity reduction
	SOC totplevel CPF	Integrated Final CPF	
Automated isolation rules	5200	5200	0x
Other CPF constructs	1600	16700	~10x
Total SOC CPF	6800	21900	~3x

PI creation cycle-time

Cycle-time for SoC PI (CPF) capture					
		Flat CPF with Netlist		Hierarchical CPF with RTL CLP	
Number of iterations		2	1	2	1
Runtime (Hrs)	Synthesis	30	15	NA	NA
	CLP	0.5	0.25	0.5	0.25
	Total	30.5	15.25	0.5	0.25

Summary

- Developed and intercepted efficient, robust, hierarchical low power design, integration, and verification methodology
  - Applied with CPF as PI format
  - Concepts and flows are generic ➔ Applicable to IEEE 1801/UPF with no or insignificant additional effort
- Early maturity of IPs before SoC ➔ Rich portfolio of reusable IPs for future SoCs
- Proven, efficient SoC power integration flow ➔ Reusable for future SoCs
- Enabled industry leading mixed-signal low power SoC with competitive power performance
- Limitations & Future scope
  - Enhancement of SoC level IPXACT® based isolation rules automation using pin power domain information
  - Full automation for manually coded simplified SoC CPF
  - Apply proposed method on a UPF based PI to identify and bridge any PI format specific gaps